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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/614,769 | 07/08/2003 | Greg Sadowski | 00100.03.0011 | 8045 |

23418 7590 05/28/2004

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

| EXAMINER | |
|---|---|
| NGUYEN, LINH M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/614,769 | SADOWSKI, GREG | |
| | Examiner | Art Unit | |
| | Linh M. Nguyen | 2816 | |

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

**Peri d f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disp sition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 16-28* is/are allowed.

6)☒ Claim(s) *8-10* is/are rejected.

7)☒ Claim(s) *11-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-28 are presented in the instant application according to the Applicants' filing on 07/08/2003.

### *Claim Objections/Minor Informalities*

1. Claims 1, 8, 14, 15, 20 and 28 are objected to because of the following informalities:

Change "capable of" to -- for --, as follows to recite positive limitations:

Claim 1, lines 4 (two occurrences), 7, 11, 16, and 17.

Claim 8, lines 3 and 4 (two occurrences).

Claim 14, lines 3, 8, 13 and 14.

Claim 15, lines 3, 8, 13 and 14.

Claim 20, lines 3, 4 (two occurrences), 11, 17, 21, 22, 23, 31, 41, 42 and 43.

Claim 28, lines 9, 13, 14, 15, 18, 23, 27, 28 and 29.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (U.S. Patent No. 6,353,906).

With respect to claim 8, Smith et al. discloses, in Figure 5, an apparatus for determining a processing speed of an integrated circuit, the apparatus comprising a) a first flip flop [104] having an input port for receiving an input signal [102], an output port for providing a flip flop

output signal [106] and a timing port for receiving an incoming clock signal [100]; b) a first delay module [108, 120] coupled to the first flip flop such that the first delay module receives the flip flop output signal, the first delay module operably coupled to receive the incoming clock signal [100] and operably coupled to receive a select delay signal [112]; and c) a second delay module [124] coupled to the first delay module such that the second delay module receives an interim timing output signal [122] from the first delay module, the second delay module operably coupled to receive the incoming clock signal, such that the second delay module generates a timing output signal [130].

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (U.S. Patent No. 6,353,906) in view of Molyneaux et al. (U.S. Patent No. 6,480,800).

With respect to claim 9, Smith et al. discloses all of the claimed limitations as expressly recited in claim 8, except for a pseudo-random input generator operably coupled to the first flip flop, such that the pseudo-random input generator generates the input signal.

Molyneaux et al. discloses, in column 3, lines 14-30, semiconductor technology, in which rigorous design verification and manufacturing testing employs pseudo-random input generators.

To configure the apparatus of Smith et al. with a pseudo-random input generator as taught by Molyneaux et al. for the capability of handling rigorous testing would have been

obvious to one of ordinary skill in the art at the time of the invention since the pseudo-random input generator could manage the sheer volume of tests with minimal problems *(see Molyneaux et al. col. 3, lines 14-30).*

With respect to claim 10, the combination of Smith et al. and Molyneaux et al. discloses a sequencer [112] *(Smith et al., Fig. 5 and col. 5, lines 56-61)* operably coupled to the multiplexer, such that the sequencer generates the select delay signal.

***Allowable Subject Matter***

6. Claims 1-7 and 16-28 are allowed if corrected to overcome the objection set forth in this office action.

7. Claims 11-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

a) An apparatus for determining a process of an integrated circuit including a multiplexer operably coupled to the at least one clock speed adjusting circuit and a delay circuit, wherein the multiplexer has a select delay input port for receiving a select delay signal such that the multiplexer generates a multiplexer output signal corresponding to at least one of an output signal generated by the at least one clock speed adjusting circuit and the delay timing signal, as called for in claims 1, 14, 15 and 20;

b) The apparatus for determining a process of an integrated circuit further comprises a logic gate coupled to the second flip flop such that the logic gate receives the timing output signal and generates a timing indicator signal, as called for in claims 11 and 12;

c) A method for determining a process of an integrated circuit including step of comparing the output timing signal with a control timing signal, in combination with the remaining claimed limitations, as called for in claim 16; and

d) A method for determining a process of a plurality of integrated circuits including the steps of repeating steps of (b) through (d) until the processing speed of the integrated circuit is determined; and recording the processing speed of the integrated circuit, as called for in claim 23.

***Citation of Relevant Prior Art***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Nakura et al. (U.S. Patent No. 6,477,186) discloses a fast operating multiplexer, in which a sum of delay times of the quarter divider and the control signal generating circuit and a setup time of the flip-flops for timing control is merely required to fall within one clock cycle, and therefore an operation speed can be high

Prior art Lee (U.S. Patent No. 6,081,462) discloses an adjustable delay circuit for setting the speed grade of a semiconductor device.

***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN